Circuit Design in Printed Complementary Organic Technologies

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Circuits based on printed OTFTs: Advantages

Technology
• Mechanical flexibility
• Simple and high-throughput (low-cost potential)
• Large-area

Application
displays, matrices of integrated sensors, RFIDs, etc
Circuits based on printed OTFTs: Challenges

- **Technology**
  - Low temperature
  - Printing techniques
  - Limited control

- **Device**
  - Global variability & mismatch
  - Defects

- **Circuits**
  - Soft faults
  - Hard faults

- State-of-the-art mainly limited to digital design and large area switch matrices
Outline

• Technology

• Modeling

• Building blocks for an RFID tag
  • Digital circuit design
  • Analog circuit design

• Conclusions
Technology

• Process

- PEN
  - Gold sputtering
  - S/D electrodes
    - SAM deposition
    - NOSC printing
  - SAM deposition

• Highlights

- Printed process
- High performance complementary OTFTs
  \( \mu_p = 1.5 \text{cm}^2/\text{Vs} \)
  \( \mu_n = 0.55 \text{cm}^2/\text{Vs} \)
- Flexible substrate
- Robust in air

S. Jacob et al., ESSDERC 2012
OTFT nominal Model

- Series of an “ideal transistor” and a reverse biased Schottky diode

p-OTFT

n-OTFT

F. Torricelli et al., ITC 2012
Statistical Model

Statistical characterization of transistor **channel** parameters

Monte Carlo simulations based on uncorrelated variations

Prediction of circuit parametric variability

50 launches of MC simulations for a Complementary inverter
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Characteristics of an p-only inverter

Cantatore et al., ISSCC 2003
Aimed application

- RFID

![Diagram of RFID system with components labeled: Reader, Tag, AM Receiver, Identity-Verification, Rectifier, Comparator, and Combinatorial and sequential logic. Arrows indicate power and data flow.]
Digital logic: combinatorial blocks

- Measurement Vs. simulation: A static NAND gate

S. Abdinia, et al, ESSCIRC 2012
Digital Circuits: Flip-flops

- A fully-static JK flip-flop

\[ f_{\text{clk}} = 100\text{Hz} \]

S. Abdinia, et al, ESSCIRC 2012
Digital Circuits: Flip-flops

- A fully-static JK flip-flop
  
  - Robust
  - Large area consumption

Prone to hard faults

$\text{f}_{\text{clk}}=100\text{Hz}$

S. Abdinia, et al, ESSCIRC 2012
Digital Circuits: Addressing area issues

- Dynamic gates $\rightarrow$ lower area

\[ f_{\text{clk}} = 150\text{Hz} \]

S. Abdinia, et al, ESSCIRC 2012
Digital Circuits: Addressing area issues

• Dynamic D Flip-flop

11 transistors compared to 36 transistors in a static MS DFF

10 times smaller
Digital Circuits: Addressing area issues

• Dynamic D Flip-flop

\[ f_{\text{clk}} = 100\text{Hz} \]

S. Abdinia, et al, ESSCIRC 2012
Analog circuits: Rectifier

- Performance Improvement:

```
Gen1
μ_p = 0.025 cm^2/Vs
μ_n = 0.023 cm^2/Vs

Gen2
μ_p = 1.5 cm^2/Vs
μ_n = 0.55 cm^2/Vs
```

S. Abdinia, et al, ESSCIRC 2012
Analog circuits: Rectifier

- Performance Improvement:

Gen1
- $\mu_p = 0.025 \text{cm}^2/\text{Vs}$
- $\mu_n = 0.023 \text{cm}^2/\text{Vs}$

Gen2
- $\mu_p = 1.5 \text{cm}^2/\text{Vs}$
- $\mu_n = 0.55 \text{cm}^2/\text{Vs}$

S. Abdinia, et al, ESSCIRC 2012
Analog circuits: Differential Comparator

- Differential OTA: measurements of 3 samples

S. Abdinia, et al, ESSCIRC 2012
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S. Abdinia, et al, ESSCIRC 2012
Analog circuits: Non-differential Comparator

- Simple offset cancelling

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S. Abdinia, et al, ESSCIRC 2012
Conclusion and future work

• In a new printed technology, agreement between simulation and measurements of several building blocks was shown, including:
  • Small-sized dynamic FF
  • Low-offset comparator (200mV)
  • 13.56MHz rectification

Realizing a fully-printed HF RFID tags is possible.
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